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K-Band High-Power GaAs FET Amplifiers

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***Abstract*—Lumped-element internal matching techniques were successfully adopted for *K*-band power GaAs FET amplifiers. The developed 18-GHz band two-stage amplifier provides 1.05-W power output at 1-dB gain compression and 1.26-W saturated power output with 8.1-dB small-signal gain. The 20-GHz band single-stage amplifier has 1.04-W power output with 3-dB associated gain. Lumped-element internal matching circuit design as well as amplifier fabrication are described. Intermodulation distortion and AM-to-PM conversion characteristics are also presented.**

I. Introduction

POWER-OUTPUT CAPABILITY for GaAs FET's has been steadily increasing. Single-stage and multistage amplifiers have already exceeded the 10-W output power level in *C*-band [1] and have exhibited multiwatt capability in *X*-band [2], [3]–[5]. Recently, in *Ku*-band high-power FET's which demonstrate 2-W output power capability have been developed [6]–[8]. High-power amplifier development in *Ku*-band and even in *K*-band, using these FET's, is now expected [6].

Above *Ku*-band, high-power FET chip width becomes comparable to the signal wavelength in a distributed-element microstrip matching circuit and it becomes much more difficult to feed a microwave signal uniformly to such a large transistor. Various parasitic reactances accompanied with FET-to-external circuit connection become appreciable and make wide-band operation of the power FET's difficult to achieve. These problems make usual distributed-element matching techniques, which were successfully used for low-noise GaAs FET amplifiers in *Ku*-, *K*-, and even *Ka*-bands [9], [10], inapplicable to high-power GaAs FET's with extremely low input impedances. These have restricted the use of GaAs FET amplifiers in *Ku*- and *K*-bands.

This paper presents effective application of lumped-element internal matching techniques to *K*-band power GaAs FET amplifiers, and microwave performances of 18- and 20-GHz band high-power FET amplifiers developed using the internal matching techniques. The developed 18-GHz band single-stage amplifier provides 1.25-W power output with 3-dB associated gain. The 20-GHz band single-stage amplifier has 1.04-W power output with 3-dB associated gain. The 18-GHz band two-stage amplifier provides 1.05-W power output at 1-dB gain compression with 8.1-dB small-signal gain and 1.25-W saturated power output.

In Section II, the device structure of NE869 series GaAs FET's and FET small-signal impedances in *K*-band are described. In Section III, lumped-element internal matching circuit design is discussed, as are amplifier fabrication and large-signal tuning. Microwave performances for the developed *K*-band single-stage and two-stage amplifiers are presented in Section IV. The effectiveness of the lumped-element internal matching techniques for FET high-power operation is demonstrated. Finally, in Section V, nonlinear distortion characteristics for the two-stage FET amplifier are discussed.

Manuscript received May 21, 1980; revised December 2, 1980. A condensed version of this paper has been presented at the 1980 IEEE-MTT-S International Microwave Symposium, Washington, D.C.
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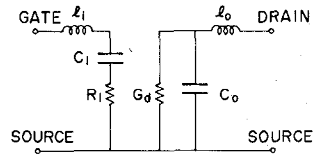

Fig. 1. RF equivalent circuit for GaAs FET input and output impedances. $l_i=0.18$ nH, $C_i=1.75$ pF, $R_i=4\Omega$, $l_o=0.17$ nH, $C_o=0.52$ pF, $G_o=10$ m℧ for NE8692.

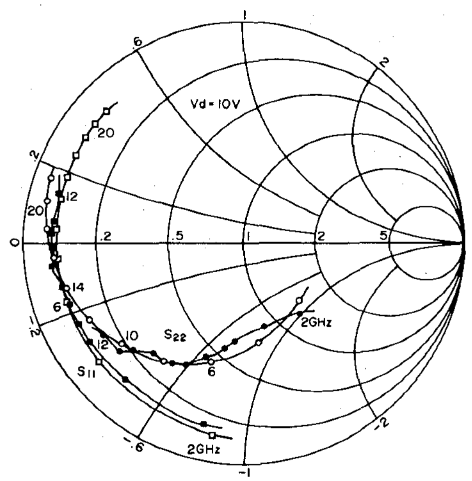

Fig. 2. GaAs FET input and output impedances. ■, ●: measured. □, ○: calculated using the FET equivalent circuit.

II. FET Small-Signal Characterization

The GaAs FET's used in the amplifier are NE869 series FET's commercially available from NEC. These FET's have graded recess structure with a submicrometer gate length Schottky barrier gate. A single chip consists of four cells and has 3-mm total gate width. The chip size is 1.14 mm wide, 0.54 mm long, and 0.12 mm thick. Typical single-cell dc characteristics are 200–220-mA saturation drain current I_{DSS}, 5.0–6.0-V pinch-off voltage V_p, and more than 20-V drain breakdown voltage [11].

It is important to know the K-band S-parameters of an FET for proper circuit design at these frequencies. However, precise measurements of the S-parameters at such high frequencies are difficult, because complicated calibration procedures are necessary with the added difficulty of realizing ideal reference standards such as "short" or "open". In order to get the S-parameters in K-band, an equivalent circuit for FET input and output impedances, based on the measured S-parameters below 12 GHz, was used. The model shown in Fig. 1 was chosen. The element values for the equivalent circuit were determined by fitting the calculated impedances with the measured impedances. The optimized element values for the NE8692-FET with 1.5-mm total gate width are also included in Fig. 1. Since the magnitude of the measured feedback parameter S_{12} is smaller than -20 dB, feedback effect S_{12} was neglected in this calculation and also in the circuit design.

The results are shown in Fig. 2, which compares measured input and output impedances for the NE8692-FET with those of the quivalent circuit. These calculated impedances are extended up to 22 GHz. All bond wires are included in these impedances as part of the FET. The impedances for large gate width FET's, such as NE8694 and NE8698, were scaled up by calculating from the impedances of the equivalent circuit for the NE8692.

From element value R_i for the NE8692 (1.5-mm total gate width), the real part for the two-chip structured NE8698 (6.0-mm total gate width) input impedance is inferred as 1 Ω. Its imaginary part becomes inductive, above Ku-band, because of the input wire inductance.

III. Matching Techniques and Amplifier Description

A. Matching Networks

Equivalent circuit topology for the lumped-element matched FET NE8698 with two-chip 6-mm total gate width structure is shown in Fig. 3. The input-matching circuit was designed, based on FET small-signal input parameter S_{11}. The lumped element input-matching circuit consists of series inductances and a parallel capacitance. The inductor is realized by a 30-μm diameter gold bonding wire. The capacitor is made on a single 0.1-mm thick ceramic substrate with a relative dielectric constant of 39. Tapered microstrip impedance-transformers with low characteristic impedances, formed on a 0.635-mm-thick alumina substrate for the 18-GHz amplifier, and formed on a 0.25-mm-thick alumina substrate for the 20-GHz amplifier, are incorporated into the lumped-element input circuits. These semilumped-element input-matching networks were effectively adopted to realize low-loss uniform-phase matching as well as wideband operation for the wide multicell and multichip structures.

The FET NE8694 single-chip 3-mm total gate width structure has an input-matching network consisting of lumped elements and a quarter-wavelength stepped transformer formed on an alumina substrate.

In order to obtain the maximum possible gain from the 20-GHz band NE8698 amplifier, values for inductances l_1, l_2 and a capacitance C in the input circuit are optimized so as to minimize the maximum value of the amplifier input VSWR in the 19 to 21-GHz range. The FET input impedance extended to K-band was used for this calculation. The optimized element values for the 20-GHz band NE8698 amplifier are $l_1=0.051$ nH, $l_2=0.06$ nH, and $C=1.0$ pF. The calculated VSWR's in the 19 to 21-GHz range are within 1.91. In this circuit design, gain rolloff in the intrinsic FET with increasing frequency (~ -6 dB/octave) was neglected, since the design of the power FET amplifier was for a relatively narrow bandwidth ($\cong 1$ GHz).

As shown in the optimization result, a series inductance with very low value ($l_1=0.05$ nH) is required to be realized in the 20-GHz band amplifier. In order to satisfy this inductance value, the capacitor on a high dielectric substrate is positioned as close to the FET chip as possible and two wires are bonded, in parallel, to each gate pad on the FET chip.

Large-signal circuit design is required for the power FET

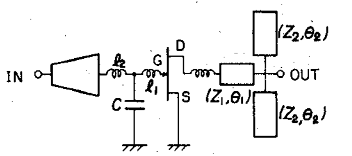

Fig. 3. Equivalent circuit for power GaAs FET amplifier. Z_1, Z_2: characteristic impedances, θ_1, θ_2: electrical lengths.

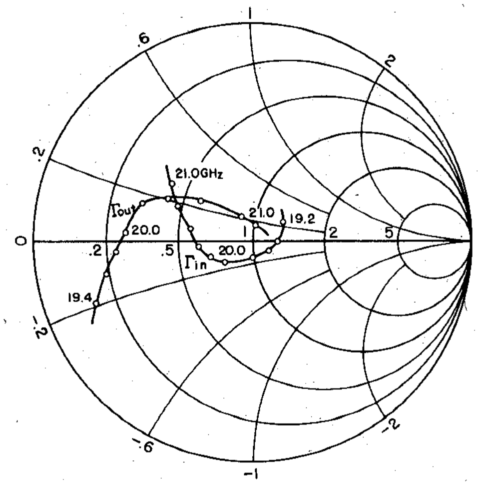

Fig. 4. Measured small-signal impedances of 20-GHz band single-stage power GaAs FET NE8698 amplifier.

output circuit. The conventional load-pull method cannot be applicable to the power transistor circuit design in such high frequencies because of difficulties of realizing the ideal impedance tuner and decoupling the FET and the circuit to measure the load impedance. In the present circuit design, the following method was adopted. The output circuit microstrip pattern in Fig. 3, with discretely movable electrical lengths θ_1 and θ_2, was formed on a 0.25-mm-thick alumina substrate. By using this output circuit as a discrete tuner, the relationship between input–output power responses and small-signal output impedances for the trial amplifier was measured. Based on these results, the optimum microstrip pattern for the output power with 3-dB associated gain was determined. The small-signal output impedances for the amplifier with the optimum output circuit are shown in Fig. 4. The maximum available gain of the FET also measured in this procedure, by tuning to the small-signal matching condition, was around 7 dB at 18 GHz.

B. Amplifier Description

Fig. 5 is a photograph of the 20-GHz band single-stage amplifier with two-chip structure. The total width of the two chips is 2.5 mm and the module is 5.7 mm long. The gate bias circuit is composed of $\lambda/4$-wavelength microstrip line and a beam-lead MIS-structured bypass capacitor. The drain bias circuit is composed of RF choke lines and a chip-type MIS-structured bypass capacitor. RF choke lines in the drain bias circuit are used because of the tolerance for large drain current density.

Fig. 6 is a photograph of the 18-GHz band two-stage amplifier, consisting of an NE8694 amplifier module as the first-stage and an NE8698 amplifier module as the second stage. Each stage amplifier module was adjusted independently and assembled on a separate carrier. DC and gate bias bypass capacitors have beam-lead MIS structures. Drain bias bypass is provided by a chip-type MIS-structured capacitor. The first-stage and the second-stage modules were interconnected by a gold tape.

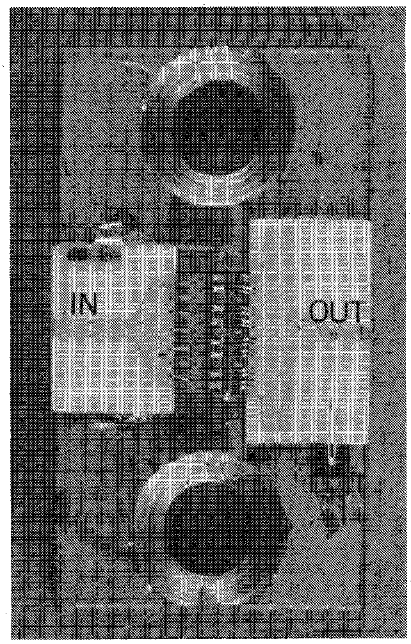

Fig. 5. 20-GHz single-stage power GaAs FET NE8698 amplifier.

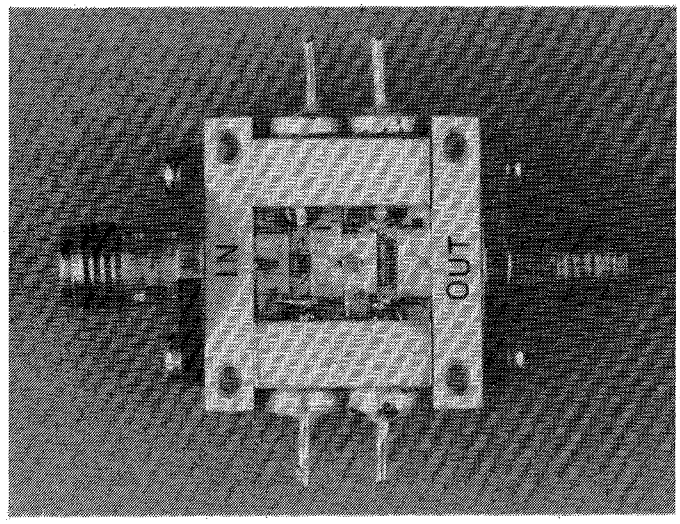

Fig. 6. Internal view of 18-GHz band two-stage power GaAs FET amplifier.

IV. Microwave Performance

The measured small-signal input and output impedances for the 20-GHz band NE8698 amplifier are shown in Fig. 4. The measurements were made using an HP K8747 transmission and reflection test unit.

The input–output responses and the power output responses versus frequency for the 18-GHz band NE8694

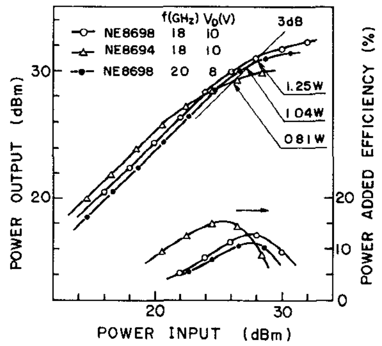

Fig. 7. Input and output responses for 18- and 20-GHz band GaAs FET amplifiers.

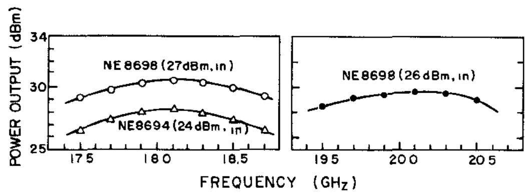

Fig. 8. Power output responses versus frequency for 18- and 20-GHz band GaAs FET amplifiers.

single-chip amplifier, the 18-GHz band NE8698 two-chip amplifier, and the 20-GHz band NE8698 two-chip amplifier are shown in Figs. 7 and 8, respectively. The 18-GHz band NE8694 amplifier has 0.8-W power output with 3-dB associated gain, 0.96-W saturated power output and 15-percent maximum power-added efficiency with 5.4-dB small-signal gain at 10-V drain voltage. The 18-GHz band NE8698 amplifier has 1.25-W power output with 3-dB associated gain, 1.68-W saturated power output, and 12.5-percent maximum power-added efficiency with 4.5-dB small-signal gain at 10-V drain voltage. The 20-GHz band NE8698 amplifier provides 1.04-W power output with 3-dB associated gain, 1.35-W saturated power output, and 11.0-percent maximum power-added efficiency with 3.8-dB small-signal gain at 8-V drain voltage. The 18-GHz band NE8698 amplifier covers the 17.7- to 18.5-GHz range with more than 1.0-W power output for 0.5-W input power level, and the 20-GHz band NE8698 amplifier covers the 19.65- to 20.5-GHz range with more than 0.8-W power output for 0.4-W input power level.

The 18-GHz band two-stage amplifier performance is shown in Fig. 9. The amplifier provides more than 0.8-W power output over the 17.7- to 18.6-GHz frequency range for 0.25-W input power level. The amplifier has 1.05-W power output at 1-dB gain compression with 8.1-dB small-signal gain, 1.26-W saturated power output, and 13.6-percent maximum power-added efficiency at 18.0 GHz.

Third-order intermodulation distortion was measured for the 18-GHz band two-stage amplifier by injecting two equal amplitude signals separated in frequency by 10 MHz and located at band center. Third-order intermodulation distortion characteristics exhibit a large gate voltage dependence, which is shown in Fig. 10. The open circles in Fig. 10 describe the intermodulation distortion ratio dependence on gate voltage V_{g1} in the first-stage amplifier module with gate voltage V_{g2} in the second-stage amplifier fixed to -3.0 V. The solid circles also show the intermodulation distortion ratio dependence on gate voltage V_{g2} with gate voltage V_{g1} fixed to -3.0 V. Both results were obtained for total output power $P_{out} = 22$ dBm. At the bias condition with small gate voltages $|V_{g1}|$ and $|V_{g2}|$, intermodulation distortion characteristics were determined. Considering these dependences on gate voltages, the gate voltages in the amplifier were fixed at relatively deep level as $V_{g1} = V_{g2} = -3.25$ V.

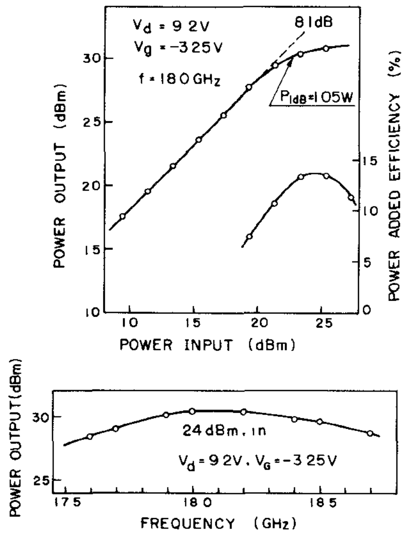

Fig. 9. Microwave performance of 18-GHz band two-stage power GaAs FET amplifier.

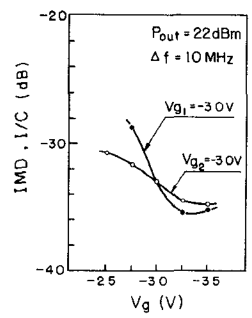

Fig. 10. Third-order intermodulation dependence on gate voltages for 18-GHz band two-stage power GaAs FET amplifier. V_{g1}: first-stage amplifier gate voltage. V_{g2}: second-stage amplifier gate voltage.

Fig. 11 shows the third-order intermodulation distortion characteristics and AM-to-PM conversion factor for the 18-GHz band two-stage amplifier. Third-order intermodulation distortion ratio was -27.5 dB at 26-dBm total power output level. The AM-to-PM conversion factor remained below 3 deg/dB for output power up to saturation.

V. Conclusion

Lumped-element internal matching techniques were successfully adopted for 18- and 20-GHz band power GaAs FET amplifiers. Single-stage and two-stage amplifiers were developed. The 18-GHz band two-stage amplifier provides 1.05-W power output at 1-dB gain compression and 1.26-W saturated power output with 8.1-dB small-signal gain. The

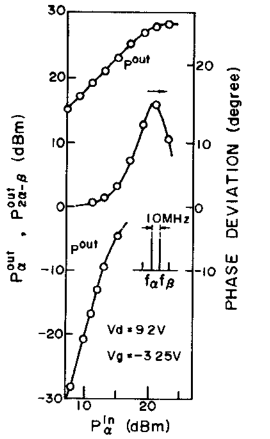

Fig. 11. Third-order intermodulation and AM-to-PM conversion characteristics of 18-GHz band two-stage power GaAs FET amplifier.

TABLE I.
MICROWAVE PERFORMANCE OF NE869 SERIES GAAS FET AMPLIFIERS. G_L: SMALL-SIGNAL GAIN. $P_{(4\ dB)}$: OUTPUT POWER WITH 4-dB ASSOCIATED GAIN. $P_{(3\ dB)}$: OUTPUT POWER WITH 3-dB ASSOCIATED GAIN. P_{sat}.: SATURATED OUTPUT POWER. W_g: GATE WIDTH.

	NE8692	NE8694	NE8698
f (GHz)	14	14	14
G_L (dB)	6.6	6 5	6 0
$P_{(4dB)}$(W)	0 53	0 96	1 9
P_{sat} (W)	0 60	1 05	2 2
Max η_{add}(%)	21 5	21 5	20 5
Wg (mm)	1 5	3 0	6 0

	NE8692	NE8694	NE8698	NE8698
f (GHz)	18	18	18	20
G_L(dB)	5.6	5.4	4 5	3 8
$P_{(3dB)}$(W)	0 42	0 83	1 25	1 04
P_{sat} (W)	0.50	0.96	1.66	1 35
Max η_{add}(%)	14 2	15 0	12 5	11 0
Wg (mm)	1 5	3 0	6 0	6 0

20-GHz band single-stage amplifier has 1.04-W power output with 3-dB associated gain.

In order to demonstrate the effectiveness of the lumped-element internal matching techniques, a summary for NE869 series FET amplifiers microwave performance is shown in Table I. For reference, the microwave performances for 14-GHz band amplifiers are quoted in this table [6]. Lumped-element internal matching techniques are adopted for large gate width FET's, such as NE8694 and NE8698. For NE8692 with relatively small gate width, distributed-element matching circuit is used.

During the first stage of this work, distributed-element matching circuits were used to develop 14-GHz band NE8694 amplifiers [12]. However, their poor power combining efficiency and resultant power gain reduction made us give up this circuit technique. On the other hand, as is shown in Table I, the high-power operation of FET's with multicell and multichip structure can be achieved by using the lumped-element internal matching techniques, without marked gain reduction and marked degradation of power combining efficiency in the large gate width FET's.

ACKNOWLEDGMENT

The authors wish to thank H. Kohzu in the Semiconductor Division for supplying power GaAs FET chips, Y. Aono, A. Higashisaka, and F. Hasegawa for developing the power GaAs FET's, and K. Ayaki and H. Katoh for their constant encouragement.

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